REMARKS

Applicant has amended claim 3 and added claim 17, and amended claim 4 and added claims 18, 19 and 20. Applicants have amended the claims in order to remove the multiple dependencies contained therein in accordance with standard U.S. practice, thereby reducing the basic filing fee. No new matter has been added to the application as a result of this amendment.

In view of the above amendments and Applicants' comments stated herein, Applicants respectfully request an early and favorable action on the merits.

Respectfully submitted,

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Marked-up Version of Claims

CLAIMS:

1. A semiconductor integrated circuit, comprising:

storing means that enables reading and writing;

comparing means that compare write data supplied to the storing means with data read from the storing means; and

variable address converting means that convert an address signal supplied to the storing means based on a comparison result in the comparing means, wherein an input signal of a logic circuit having a desired logical function is input as the address signal to the storing means, and wherein the data is written to the storing means so that the read data of the storing means can be obtained as an expected output signal with respect to the input signal of the logic circuit.

2. A semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.

3. A semiconductor integrated circuit according to claim 1 ~~or 2~~, wherein the storing means are a volatile memory.

4. A semiconductor integrated circuit according to claim 1, ~~2, or 3,~~ wherein the variable address converting means comprise: a memory array in which a plurality of memory cells